ABSTRACT

This invention relates to a memory device and the like that are preferably applied to a case where motion vector is detected using a block matching. Pixel data of a first frame (a reference frame) is stored in a unit A of memory cell array portion 20a in straight binary format. Pixel data of a second frame (a search frame) is stored in a unit B of memory cell array portion 20b in two's complement format. The units A and B have a plurality of memory cells, respectively. Word lines WL related to the pixel data of the first and second frames are simultaneously activated so that charges accumulated in capacitors of each of the memory cells can be combined along one bit line BL. A/D converter 53 outputs a digital signal (absolute difference value) having a value that corresponds to a total amount of charges. When reading the pixel data, a subtraction and a conversion into the absolute difference value are simultaneously performed.